AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A disk array apparatus comprising:

a cache memory ~~for~~ that temporarily ~~storing~~ stores data to be read from or written to disks; and

a control unit which associates data associated with logical addresses with physical addresses, writes the data associated with physical address in the cache memory and processes preferentially for writing the data associated with the physical addresses in the cache memory to the disks;

wherein said disks include a first disk and a second disk; and wherein said control unit processes first data to be read from or written to said first disk with a timing determined in relation to reading or writing of second data to said second disk.

2. (original) The disk array apparatus as claimed in claim 1, wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed.

3. (original) The disk array apparatus as claimed in claim 1, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory.

4. (original) The disk array apparatus as claimed in claim 1, wherein said cache memory is a nonvolatile memory.

5. (original) The disk array apparatus as claimed in claim 2, wherein said cache memory is a nonvolatile memory.

6. (original) The disk array apparatus as claimed in claim 3, wherein said cache memory is a nonvolatile memory.

7. (currently amended) A data writing method in a disk array apparatus for reading and writing data from and to a plurality of disks in accordance with a command issued from an upper-level host computer, the method comprising ~~the steps of~~:

before executing a processing for writing data to the plurality of disks, associating data associated with logical addresses with physical addresses to be temporarily stored in a cache memory;

associating data associated with logical addresses with physical addresses;

writing the data associated with physical address in the cache memory; and

processing preferentially for writing the data

associated with the physical addresses in the cache memory to the disks;

wherein first data associated with the physical addresses in the cache memory is read to or written from a first of said plurality of disks with a timing determined in relation to reading or writing second data associated with the physical addresses in the cache memory to or from a second of said plurality of disks.

8. (currently amended) The data writing method as claimed in claim 7, further comprising ~~the step of~~:

releasing the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed.

9. (original) The data writing method as claimed in claim 7, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein, if a failure occurs in one control unit, another control unit takes over the preference processing for the data associated with a physical address in the cache memory.

10. (original) The data writing method as claimed in claim 8, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein, if a failure occurs in one control unit, another control unit takes over the preference processing for the data associated

with a physical address in the cache memory.

11. (new) A disk array apparatus comprising:

a cache memory that temporarily stores data to be read from or written to a plurality of disks; and

a control unit which associates data associated with logical addresses with physical addresses, writes the data associated with physical address in the cache memory and processes preferentially for writing the data associated with the physical addresses in the cache memory to the disks;

wherein the data associated with the physical addresses comprises new data to be written at least to a first disk, and new check information to be written at least to a second disk that is different than said first disk.

12. (new) The disk array apparatus as claimed in claim 11, wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed.

13. (new) The disk array apparatus as claimed in claim 11, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory.

14. (new) The disk array apparatus as claimed in claim

11, wherein said cache memory is a nonvolatile memory.

15. (new) The disk array apparatus as claimed in claim 12, wherein said cache memory is a nonvolatile memory.

16. (new) The disk array apparatus as claimed in claim 13, wherein said cache memory is a nonvolatile memory.